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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,597	12/31/2001	Howard S. David	42390.P13871	2206

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2186	8

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PRC

Office Action Summary	Application No	Applicant(s)	
	10/039,597	DAVID, HOWARD S.	
	Examiner	Art Unit	
	Zhuo H Li	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office action is in response to the amendment filed on January 21, 2004 (Paper no. 7)

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stracovsky et al. (US PAT. 6,216,178 hereinafter Stracovsky) in view of Saulsbury et al. (US PAT 6,128,702 hereinafter Saulsbury).

Regarding claim 1, Stracovsky discloses a memory controller, i.e., universal controller (104, figure 1B) comprising a plurality of tag units, resource tags (114, figure 1B), each tag unit including an array of tag address storage location, the plurality of tag units (300, figure 3A and 308, 310 in figure 3B) to perform tag look-up operation associated to the data stored in the memory (108, figure 1B) and (col. 7 line 24 through col. 8 line 32), a command sequencer and serializer unit, i.e., command sequencer (116, figure 1B) coupled to the array of tag address storage locations to determent the state of requested data located in the memory (108, figure 1B), the command sequencer unit to control the memory via the memory bus (220, figure 1B), and a

memory module decode unit, i.e., configurable system interface (110, figure 1B), and the memory module decode unit to perform decode operations in parallel with the tag look-up operations (col. 6 line 21 through col. 7 line 10). Stracovsky differs from the claimed invention in not specifically teaches a plurality of data caches located on one of the plurality of memory modules, and a memory module decode unit, the memory module decode unit to perform decode operations in parallel with the tag look-up operations. However, Saulsbury teaches the computer system (100, figure 1) comprising a plurality of memory blocks (104, figure 1) in the memory system (103, figure 1) is able to read and write data from the controller, i.e., CPU (102, figure 1) via a plurality of command and data buses, in addition, each of the memory block comprising a main memory bank (118, figure 1) and a primary data cache (122, figure 1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the system of Stracovsky in having a plurality of data caches located on one of the plurality of memory modules, as per teaching by the system of Saulsbury, because it reduces the miss rate and increase the access speed of in the memory operation.

Regarding claims 2-3, Stracovsky discloses each of the plurality of tag units corresponding to one of the plurality of memory modules and the tag look-up operations to provide cache hit information (col. 7 line 24 through col. 8 line 32)

Regarding claim 4, Stracovsky discloses the tag look-up operations to provide cache line modified information (col. 9 lines 2-66).

Regarding claim 5, Saulsbury discloses each of the arrays of tag address storage locations organized into a plurality of ways (col. 3 lines 54-63).

Regarding claim 6, Saulsbury discloses the tag look-up operations to provide way information (col. 12 line 48 through col. 13 line 66 and col. 14 lines 37-64).

Regarding claim 7, Saulsbury discloses each of the arrays of tag address storage locations organized into 4 ways (col. 3 lines 54-63).

Regarding claim 8, Stracovsky discloses the command sequencer (116, figure 1B) to control the plurality of data caches located on the memory as defined in claim 1 above, and the command sequencer control the plurality of memory modules (device type 1 – device type N, figure 1C) by delivering commands over the memory bus (220, figure 1B), the memory bus including a plurality of command and address lines (figure 1C and col. 7 line 39 through col. 8 line 2 and col. 11 line 50 through col. 12 line 19).

Regarding claim 9, Stracovsky discloses the plurality of command and address lines are part of a point-to-point interconnect (figure 9 and col. 11 line 50 through col. 13 line 4).

Regarding claim 10, Stracovsky discloses a system (100, figure 1B) comprising a processor (102, figure 1B), a memory controller (104, figure 1B) coupled to the processor via the system bus (106, figure 1B), the memory controller including a plurality of tag units (114, figure 1B), each tag unit including an array of tag address storage locations, the plurality of tag units (300, figure 3A and 308, 310 in figure 3B) to perform tag look-up operation associated to the data stored in the memory (108, figure 1B) and (col. 7 line 24 through col. 8 line 32), a memory module decode unit, i.e., configurable system interface (110, figure 1B), and the memory module decode unit to perform decode operations in parallel with the tag look-up operations (col. 6 line 21 through col. 7 line 10), a command sequencer and serializer unit (116, figure 1B) coupled to the array of tag address storage locations, and a plurality of memory modules, i.e., device type 1

– device type N, in figure 1C, coupled to the memory controller via a memory bus (220, figure 1B). Stracovsky differs from the claimed invention in not specifically teaches the memory modules including a memory device and a data cache coupled to the memory device, the data cache controlled by commands delivered by the memory controller. However, Saulsbury teaches the computer system (100, figure 1) comprising a plurality of memory blocks (104, figure 1) in the memory system (103, figure 1) is able to read and write data from the controller, i.e., CPU (102, figure 1) via a plurality of command and data buses, in addition, each of the memory block comprising a main memory bank (118, figure 1) and a primary data cache (122, figure 1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the system of Stracovsky in having the memory modules including a memory device and a data cache coupled to the memory device, the data cache controlled by commands delivered by the memory controller, as per teaching by the system of Saulsbury, because it reduces the miss rate and increase the access speed of in the memory operation.

Regarding claim 11, the limitations of the claim are rejected as the same reasons set forth in claim 9.

Regarding claim 12, Saulsbury discloses the arrays of tag address storage locations and the data caches organized into a plurality of ways (col. 3 lines 54-63).

Regarding claim 13, the limitations of the claim are rejected as the same reasons set forth in claim 2-3.

Regarding claim 14, the limitations of the claim are rejected as the same reasons set forth in claim 4.

Regarding claim 15, the limitations of the claim are rejected as the same reasons set forth in claim 6.

Regarding claim 16, Stracovsky disclose a method comprising receiving a read request at a memory controller (104, figure 1B) from the processor (102, figure 1B) via the system bus (106, figure 1B), performing a tag look-up within the memory controller to determine whether there is hit for the read request in the memory module (108, figure 1B) via the resource (114, figure 1B) and the look-up unit table (118, 1B) which are both located in the memory controller (col. 7 line 25 through col. 8 line 32 and col. 9 lines 2-66), determining which of a plurality of memory modules (device type 1 – device type N, figure 1C) is addressed by the read request, wherein performing a tag look-up and determining which of a plurality of memory modules is addressed by the read request occur in parallel, and fetching a line of data from the plurality of memory modules if the tag look-up indicates a hit (col. 13 line 8 through col. 14 line 13), the memory modules separate from the memory controller and coupled to the memory controller via a memory bus (220, figure 1B). Stracovsky differs from the claimed invention in not specifically teaches the data cache located on each of the memory module. However, Saulsbury teaches the computer system (100, figure 1) comprising a plurality of memory blocks (104, figure 1) in the memory system (103, figure 1) is able to read and write data from the controller, i.e., CPU (102, figure 1) via a plurality of command and data buses, in addition, each of the memory block comprising a main memory bank (118, figure 1) and a primary data cache (122, figure 1). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the system of Stracovsky in having the memory modules including a data cache coupled to the memory device, the data cache controlled by commands

delivered by the memory controller, as per teaching by the system of Saulsbury, because it reduces the miss rate and increase the access speed of in the memory operation.

Regarding claim 17, the limitations of the claim are rejected as the same reasons set forth in claim 6.

Regarding claim 18, the limitations of the claim are rejected as the same reasons set forth in claim 4.

Response to Arguments

4. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H Li whose telephone number is 703-305-3846. The examiner can normally be reached on Tue-Fri 9:00 a.m. to 6:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 703-305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zhuo H. Li

March 19, 2004

MATTHEW KIM
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